

FIG. 1A

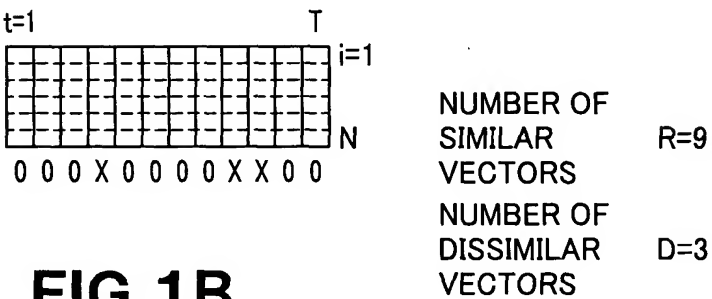
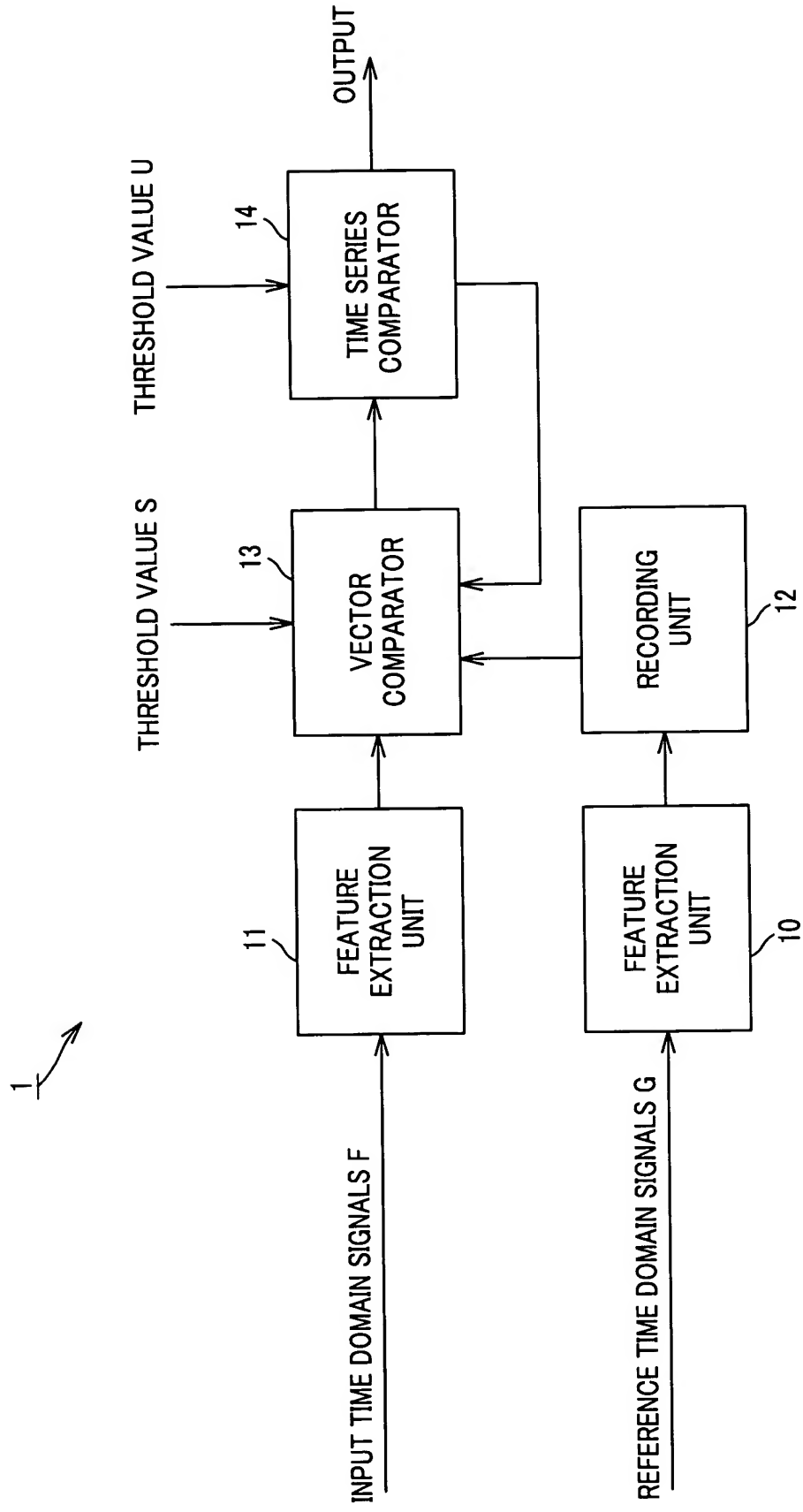
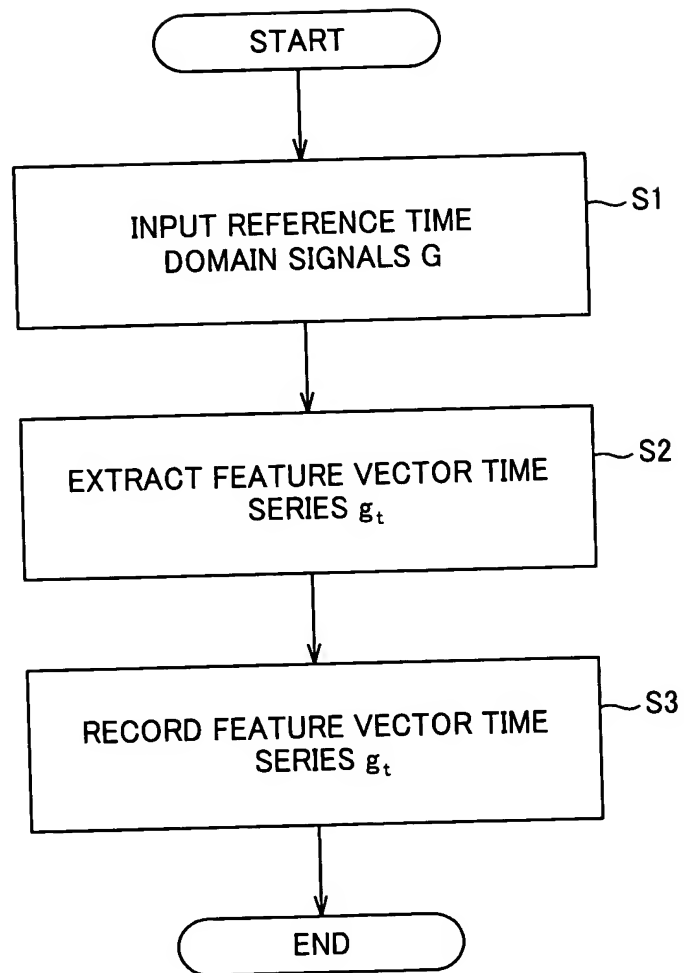


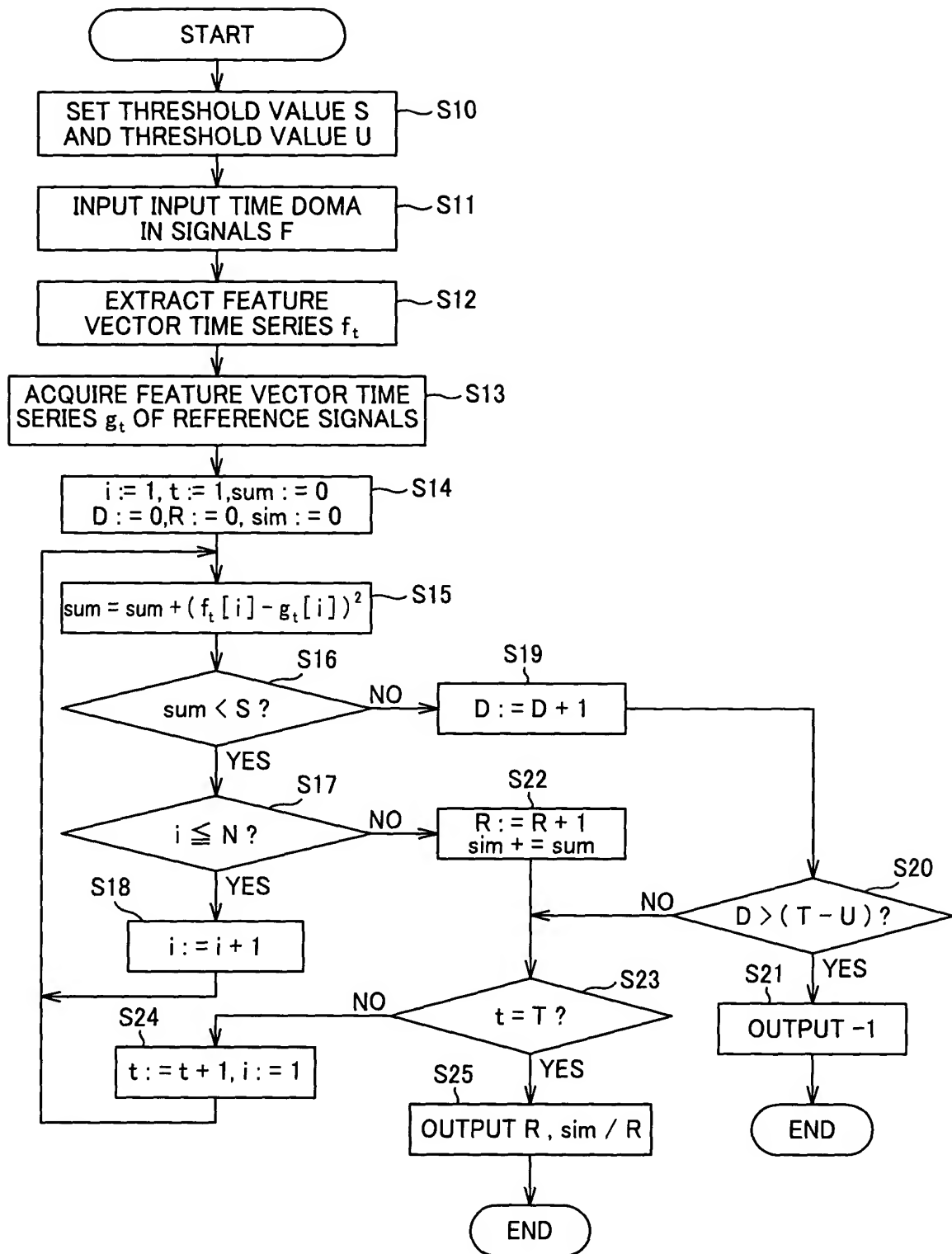
FIG. 1B



**FIG.2**

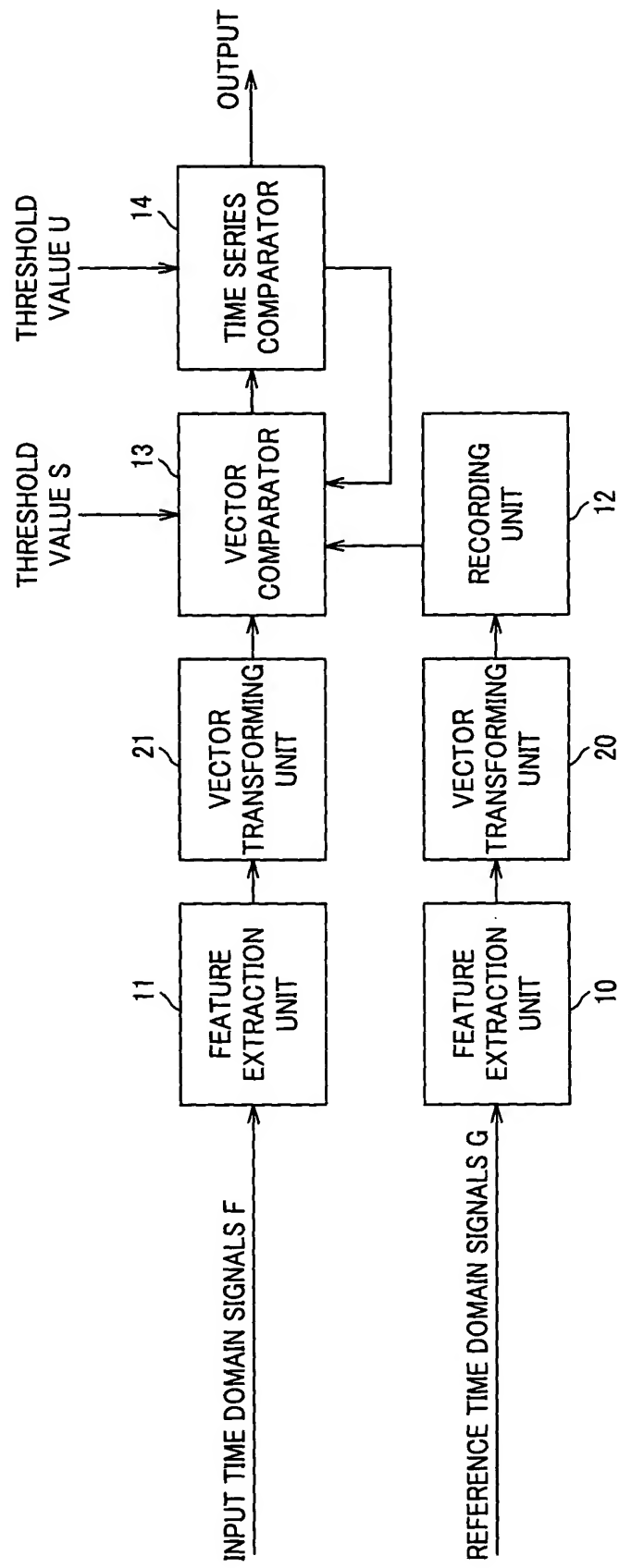


**FIG.3**



**FIG.4**

2 ↗



**FIG.5**

3 ↗

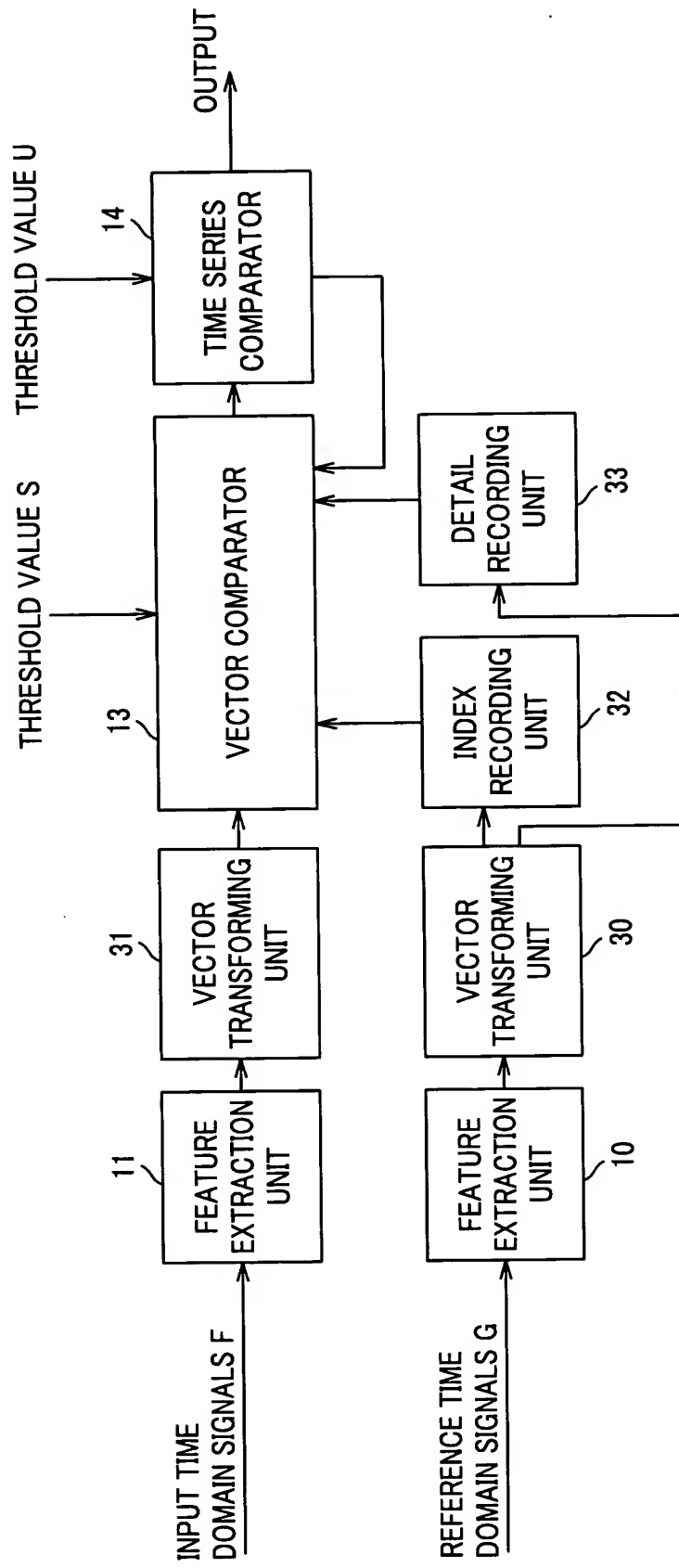
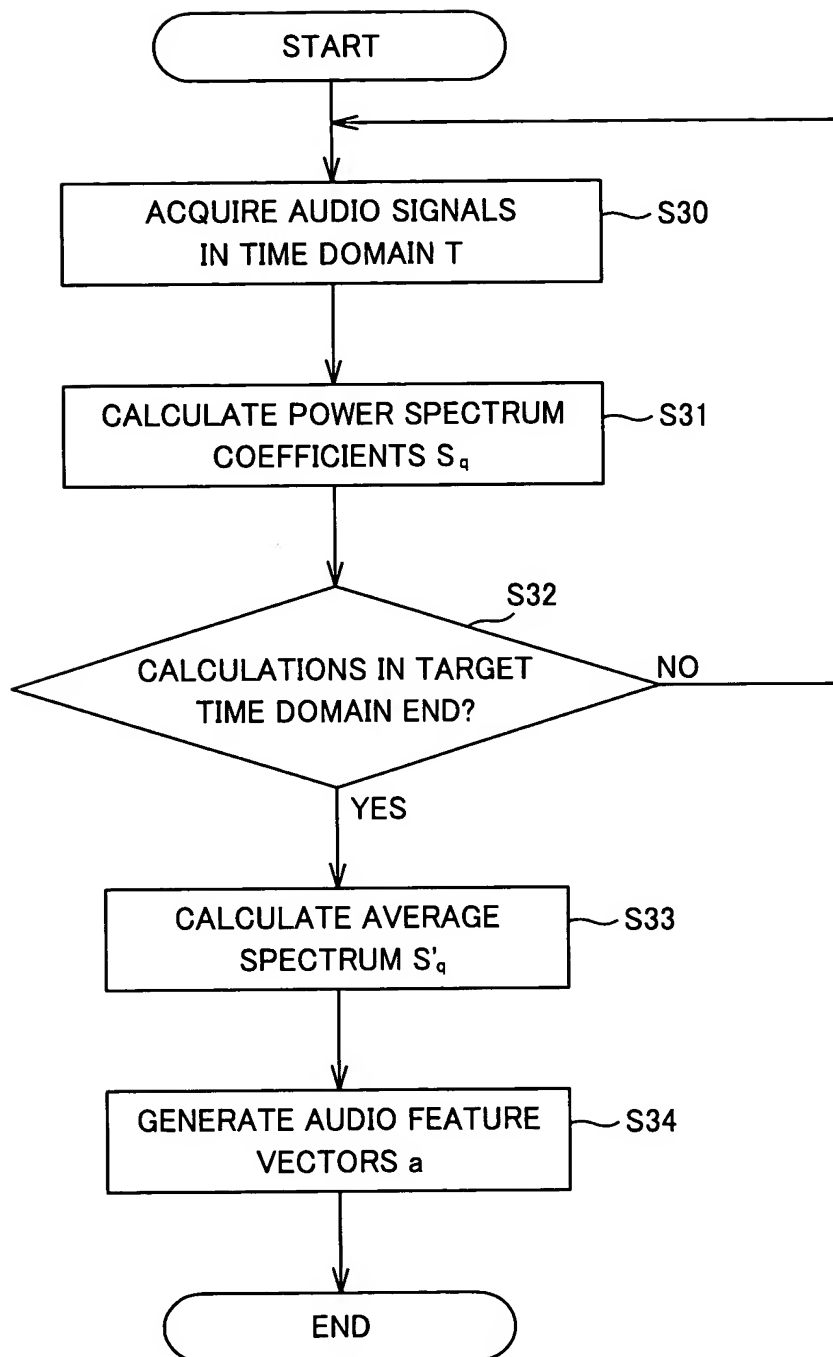
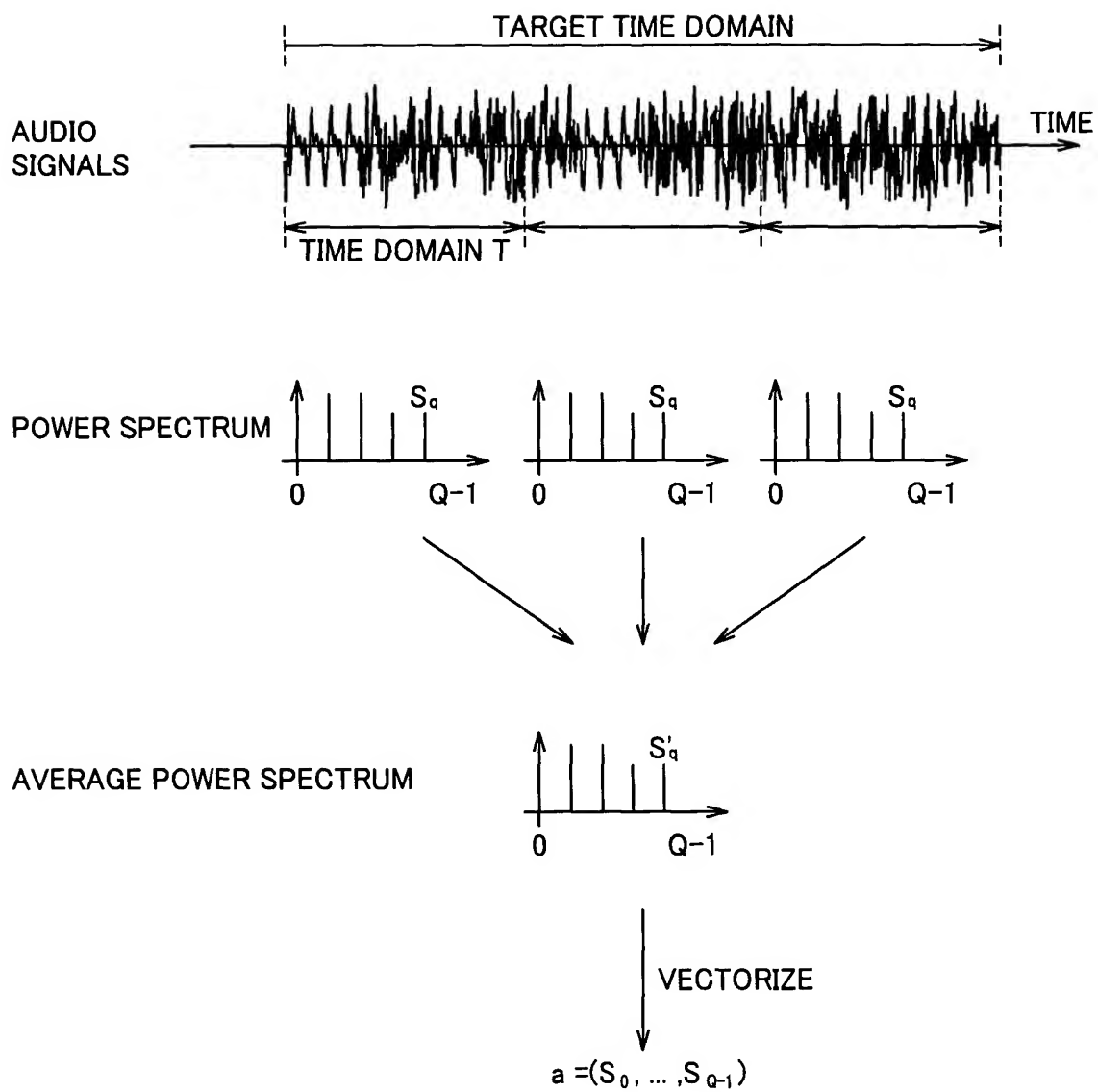


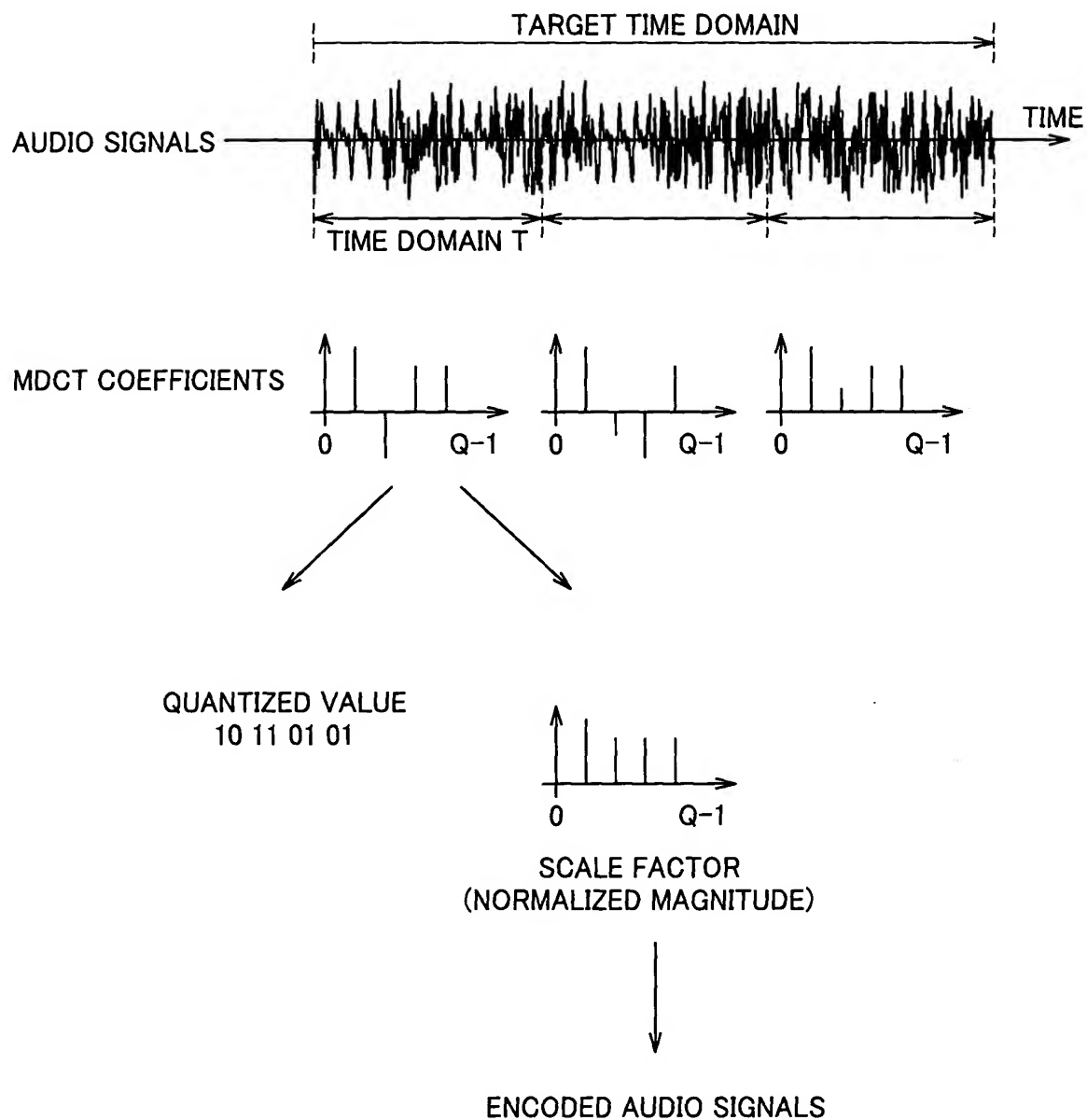
FIG. 6



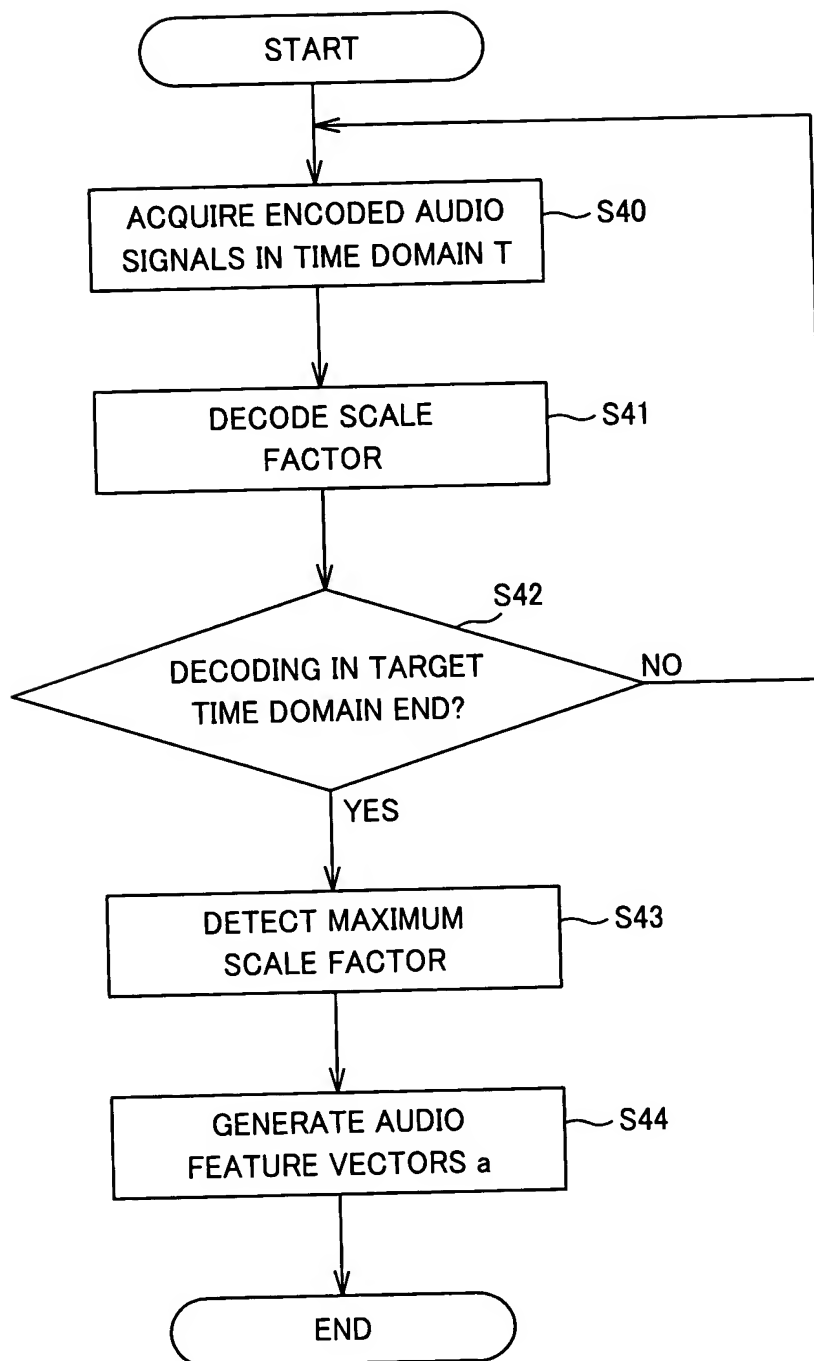
**FIG.7**



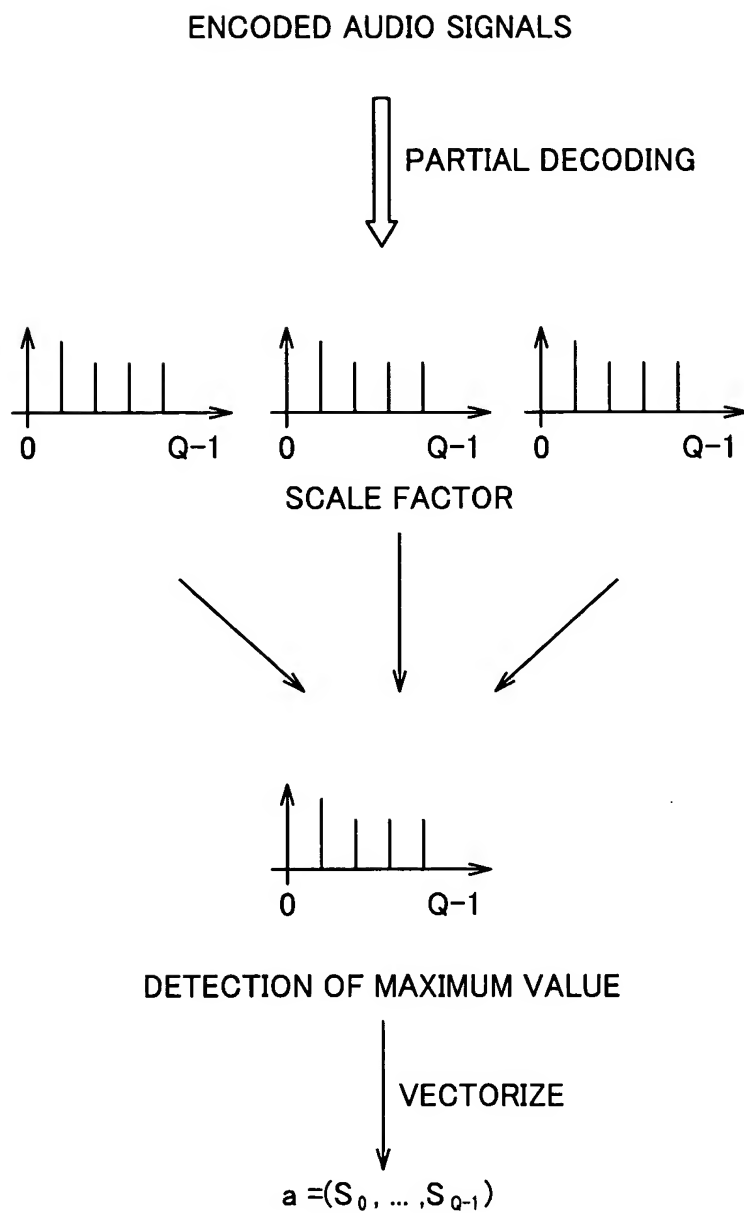
**FIG.8**



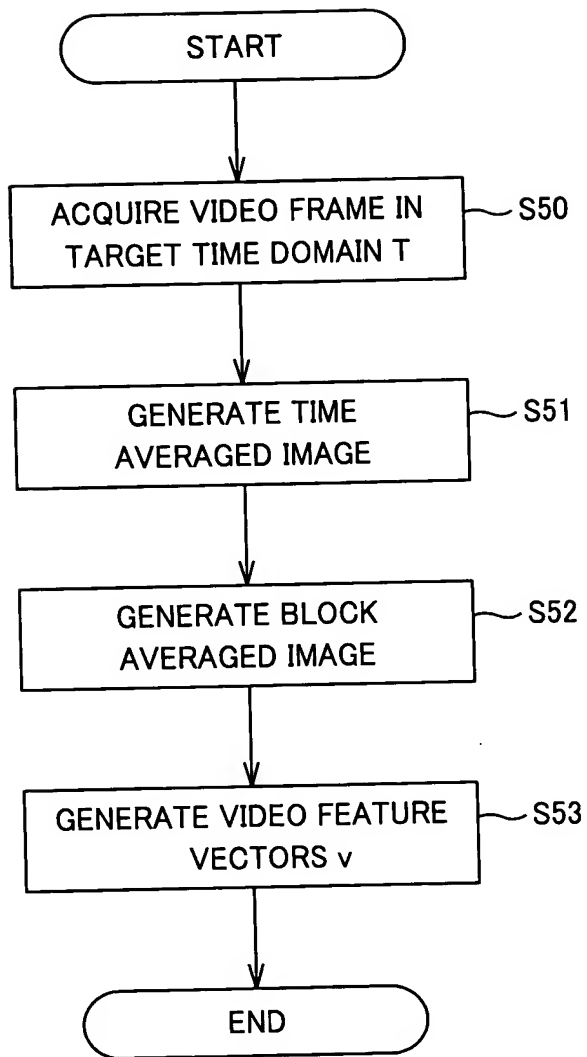
**FIG.9**



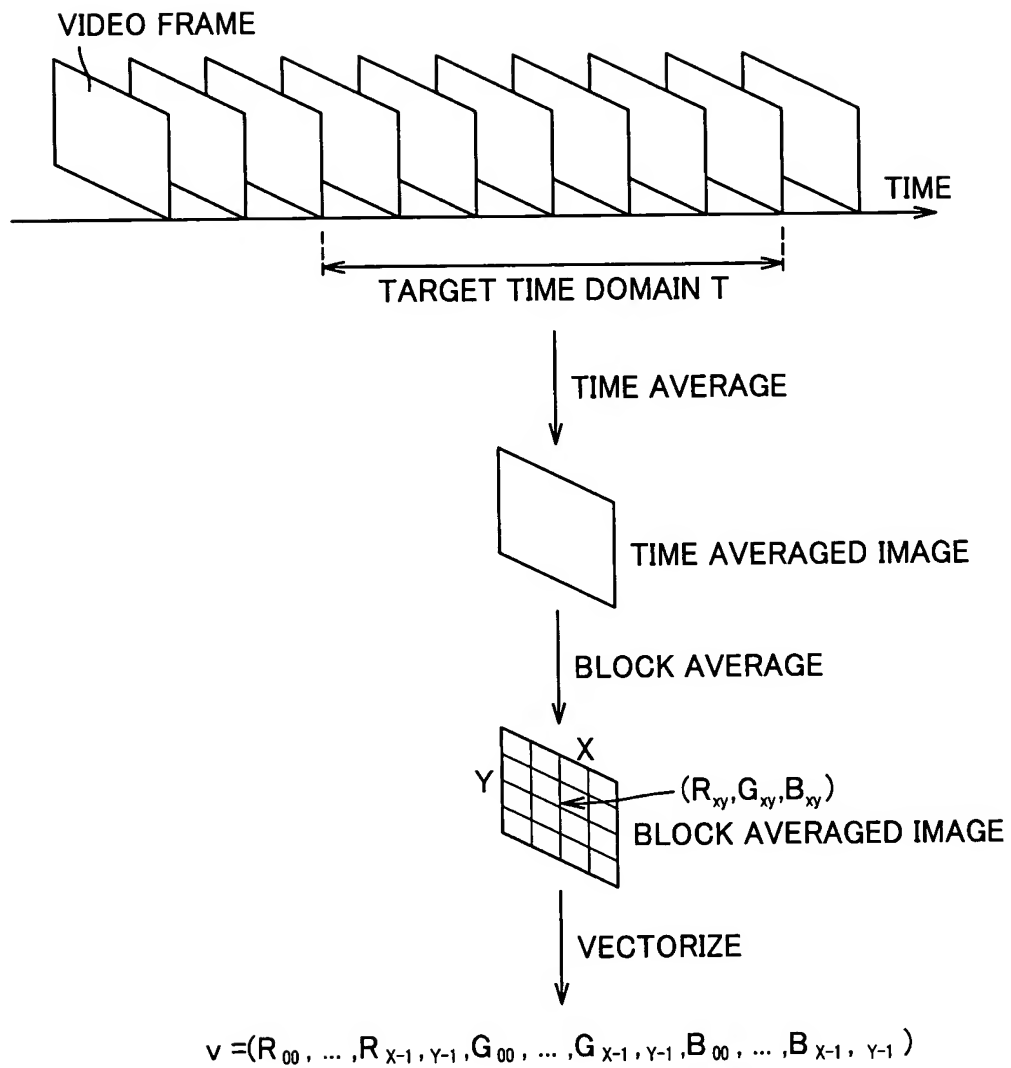
**FIG.10**



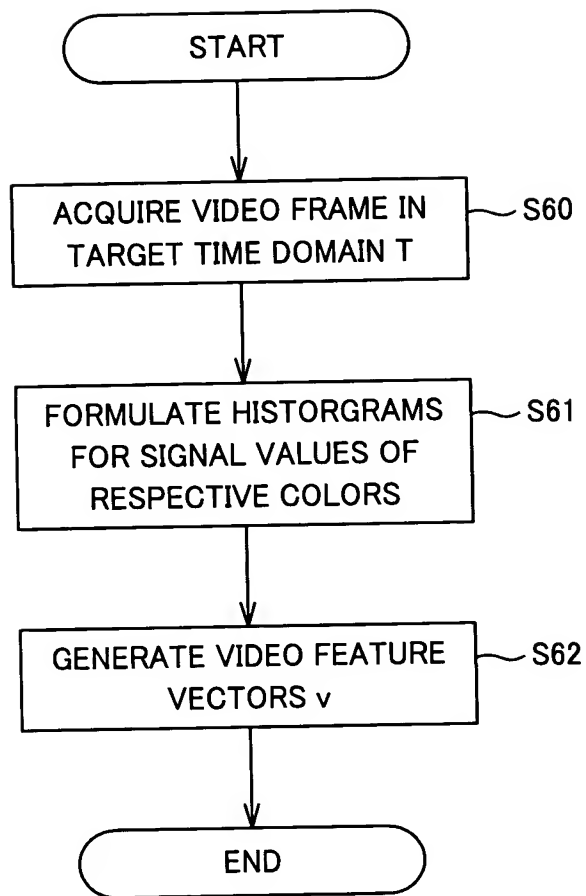
**FIG.1 1**



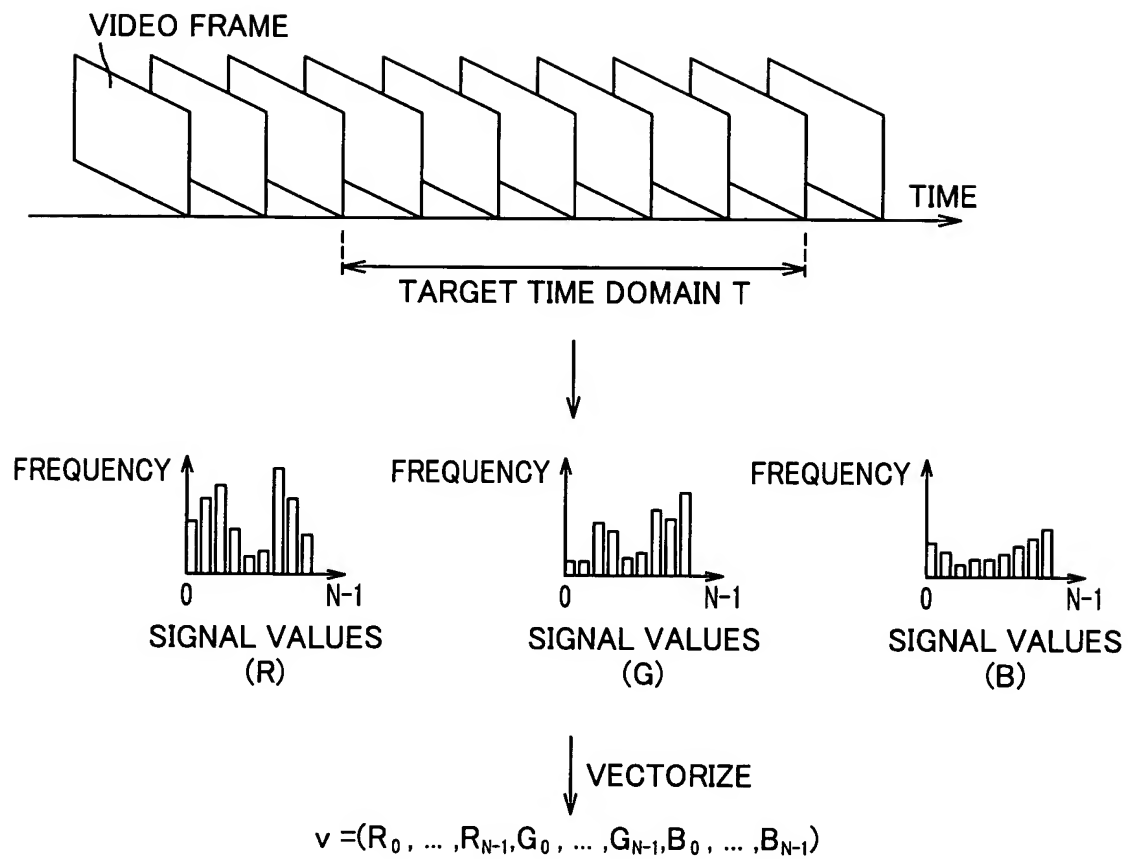
**FIG.12**



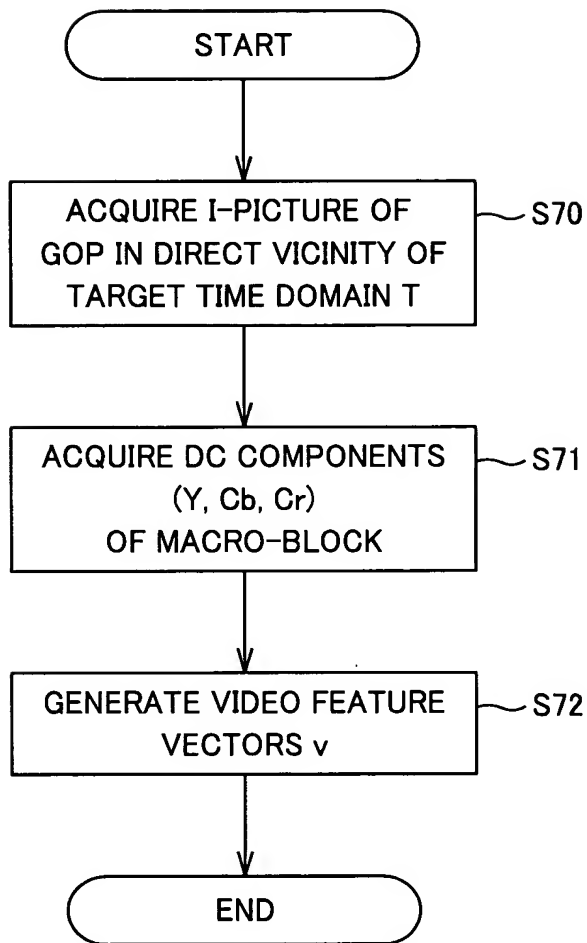
**FIG.13**



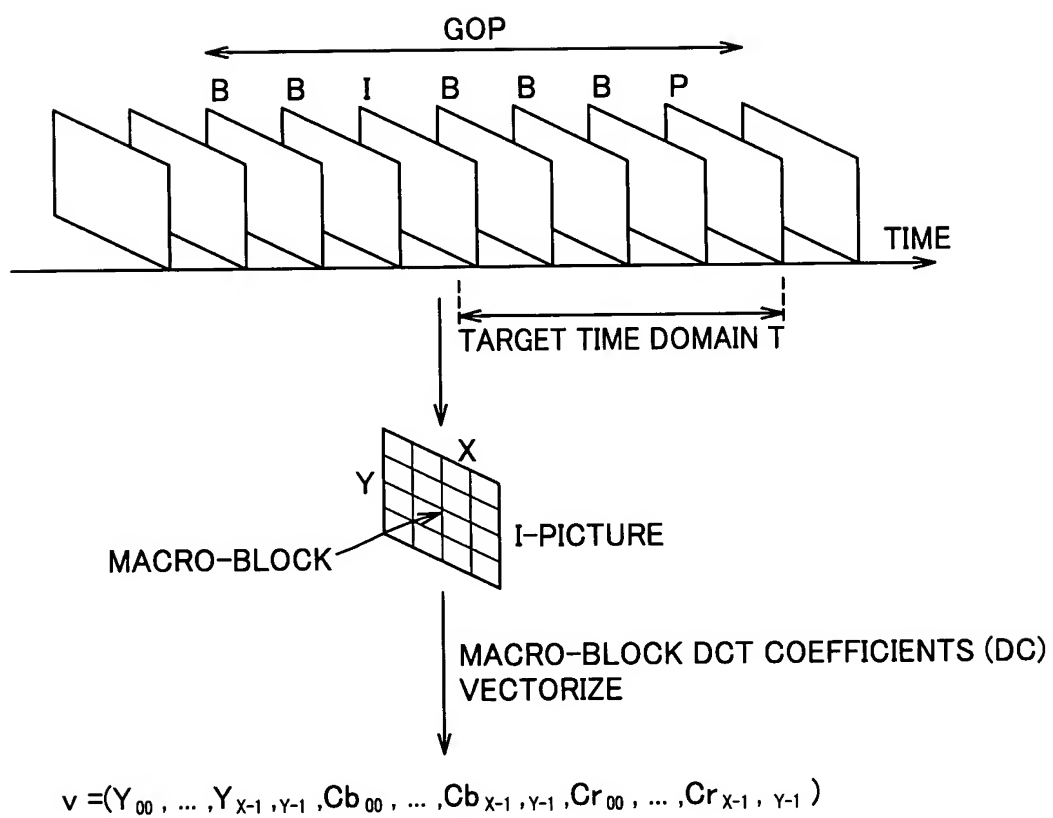
**FIG.14**



**FIG.15**

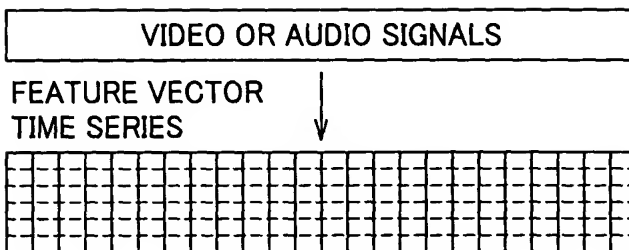


**FIG.16**

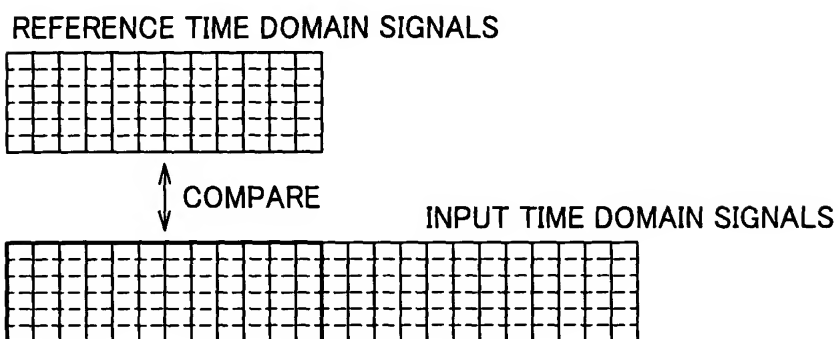


**FIG.17**

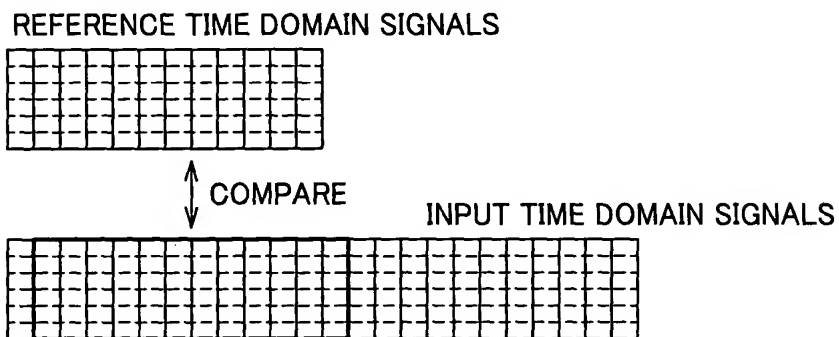
**FIG. 18A**



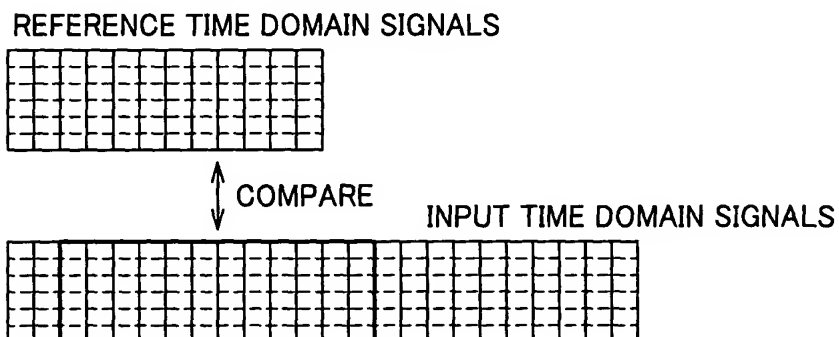
**FIG. 18B**



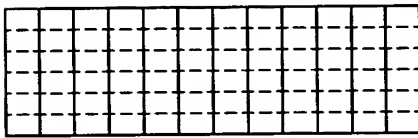
**FIG. 18C**



**FIG. 18D**

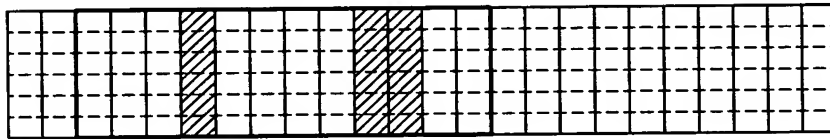


REFERENCE TIME DOMAIN SIGNALS



COMPARE

INPUT TIME DOMAIN SIGNALS



**FIG. 19**